

## CLAIMS

[1] A cache memory comprising:

a flag holding unit which holds, in a correspondence with a cache entry which holds a data unit of caching, a valid flag indicating whether or not the cache entry is valid, and a dirty flag indicating whether or not the cache entry has been written into; and

an altering unit operable to alter, based on an command from a processor, at least one of the valid flag and the dirty flag, contrary to the state of the cache entry.

[2] The cache memory according to Claim 1,

wherein said altering unit is operable to set, in the cache entry, an address serving as a tag, and to set the valid flag, without loading data from a memory.

[3] The cache memory according to Claim 2,

wherein said altering unit is operable to reset the dirty flag of the cache entry in a state in which the cache entry holds rewritten data that has not been written back.

[4] The cache memory according to one of Claim 2 and Claim 3, further comprising:

a holding unit which holds an address range specified by the processor; and

an identification unit operable to identify a cache entry which holds data belonging to the held address range,

wherein said altering unit is operable to alter at least one of the valid flag and the dirty flag of the identified cache entry.

[5] The cache memory according to Claim 4,

wherein said identification unit includes:

a first conversion unit operable, in the case where a start

address of the address range indicates a point midway through line data, to convert the start address into a start line address indicating a start line included in the address range;

a second conversion unit operable, in the case where an end address of the address range indicates a point midway through the line data, to convert the end address into an end line address indicating an end line included in the address range; and

a judgment unit operable to judge whether or not there exist cache entries which hold data corresponding to respective line addresses from the start line address to the end line address.

[6] The cache memory according to Claim 1,  
wherein said altering unit includes:

an instruction detection unit operable to detect execution of a memory access instruction having a dirty flag reset directive; and

a flag rewriting unit operable to reset a dirty flag of a cache entry which is accessed according to the instruction.

[7] The cache memory according to Claim 1,  
wherein said altering unit includes:

an instruction detection unit operable to detect execution of a memory access instruction having a valid flag reset directive; and

a flag rewriting unit operable to reset a valid flag of a cache entry which is accessed according to the instruction.

[8] A method for controlling a cache memory having, in a correspondence with a cache entry which holds a data unit of caching, a valid flag indicating whether or not the cache entry is valid, and a dirty flag indicating whether or not the cache entry has been written into, the cache entry holding a data unit of caching, said method comprising:

a step of setting, in the cache entry, an address serving as a

tag, and setting the valid flag, without loading data from a memory, based on a command from the processor; and

a step of resetting, based on a command from the processor, the dirty flag of the cache entry in a state in which the cache entry

5 holds rewritten data that has not been written back.